

REMARKS

Claims 1, 4, 9, 12, 13, 17 and 18 have been amended. Claims 1 to 20 remain active in this application of which claims 5, 13 and 18 to 20 were allowed in their prior state.

The specification has been amended to clarify the problem astutely raised by the examiner. No new matter has been added because the revised portion of the specification in the revised form is fully readable upon the drawings as originally filed. The error appears to be in inaccurately describing a first order filter as a second order filter as noted by the examiner. This has been corrected.

For the record, it should be noted that elements 14 and 24 provide a first order switched capacitor (SC) filter for the feedback path and elements 12 plus 14 plus 24 provide the input signal path as a first order SC filter. Element 26 is the continuous time (CT) first order filter. There is no stand alone second order filter. In other words, for quantization noise, filter 14/24 is a first order SC filter and filter 26 is a first order CT filter. For the input signal, element 12 plus filters 14/24 are a first order SC filter and filter 26 is a first order CT filter. Note that element 12 can be replaced by a resistor (page 6, line 28).

Claims 1 to 20 were objected to because the passive filter providing a first order and a second order filter in not commensurate with the description. The objection is believed to be overcome in view of the amendment to the specification which is explained above.

Claims 1 to 4, 6 to 12, and 14 to 17 were rejected under 35 U.S.C.103(a) as being unpatentable over the Benabes et al. article in view of the Chan article and Yamakido et al. or Voorman et al. The rejection is again respectfully traversed.

The arguments previously presented are repeated. In addition, it is noted that the claims required that the continuous time circuit not only be passive, but that it contain both capacitors and resistors. Clearly, Benabes nowhere teaches or suggests the circuit as claimed either in structure format or in method format other than stating that a design for a passive sigma-delta converter is provided. The claims herein require much more. As to the Chen reference, no resistive elements are shown in any of the circuits depicted.

In addition, the claims require the combination of the passive continuous time circuit in combination with a passive discrete time stage wherein the input signal and the feedback signal are combined. There is no teaching or suggestion in any of the references not only of such a circuit, but of such a combination. While the individual circuits depicted may be in the prior art, the combination as claimed is nowhere taught or suggested,

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,



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